WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, including the steps of:

providing a substrate having first and second main surfaces and having a semiconductor element formed in the first main surface;

forming a first groove in the first main surface of the substrate, the first groove having a bottom surface with a width and opposing side surfaces on the bottom surface;

forming selectively a catalyst layer on the bottom surface of the first groove, the catalyst layer containing palladium in an upper surface thereof;

forming a fist metal layer of a nickel based plating layer on the upper surface of the catalyst layer by an electroless plating technique, a top portion of the first metal layer located at a distance below a top end of the side surface of the first groove;

forming a second groove in the second main surface of the substrate along the first groove, the second groove having a bottom with a smaller width than that of the bottom of the first groove and opposing side surfaces on the bottom surface, the bottom surface of the second groove being a backside surface of the catalyst layer;

forming a second metal layer overlying the bottom

and side surfaces of the second groove; and

laser-cutting the first metal layer, the catalyst layer, and the second metal layer through the first groove.

2. A method for manufacturing a semiconductor device according to claim 1, after the step of forming the first metal layer further comprising the step of:

attaching a supporting member on the first main surface, and thinning the substrate through the second main surface.

3. A method for manufacturing a semiconductor device according to claim 1, wherein the step of forming the catalyst layer containing the steps of:

forming a first photoresist layer on the first surface of the substrate, the photoresist layer having an opening opposing to the first groove;

depositing a catalyst material on the bottom surface of the first groove through the first photoresist layer as a mask by evaporation or sputtering deposition; and

removing the first photoresist layer together with the catalyst material on the photoresist layer, and remaining the catalyst material on the bottom surface of the first groove.

4. A method for manufacturing a semiconductor device according to claim 1, wherein the catalyst layer has

two-layers of a palladium layer and a titanium layer under the palladium layer, or a single palladium layer.

5. A method for manufacturing a semiconductor device according to claim 1, wherein the nickel based plating layer is made of one material selected from Ni-P alloy, Ni-B alloy, and Ni-B-W alloy.

6. A semiconductor device, comprising:

a semiconductor substrate having first and second main surfaces, having a semiconductor element formed in the first main surface and having a peripheral surface containing the first and second main surface;

a heat radiation layer provided on the second main surface of the semiconductor substrate; and

a flange of a plurality of metal layers disposed on the peripheral surface of the substrate, the metal layers comprising;

a first metal layer having a surface layer containing palladium on the same side with the first main surface,

a second metal layer of nickel based alloy disposed on the surface layer containing palladium of the first metal layer, and the second metal layer having a top portion located at a distance below the first main surface, and

a third metal layer disposed under the first

metal layer.

7. A semiconductor device according to claim 6, wherein the third metal layer comprises a nickel based alloy layer, a gold layer and a laser-cut metal layer including a nickel layer or a chromium layer.

8. A semiconductor device according to claim 7, wherein the third metal layer further comprises a single layer of gold or a plurality of layers including a titanium layer and a gold layer on the laser-cut metal layer.

9. A semiconductor device according to claim 6, wherein the first metal layer comprises two-layers of a palladium layer and a titanium layer under the palladium layer, or a single layer.

10. A semiconductor device according to claim 6, wherein the second metal layer is made of one material selected from Ni-P alloy, Ni-B alloy, and Ni-B-W alloy.